Rigorous Analysis and Design of a High-Performance 94 GHz MMIC Doubler

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Abstract—A 94 GHz monolithic microwave integrated circuit (MMIC) frequency doubler with 25 percent efficiency and 65 mW output power has been developed using Schottky-barrier varactor diode. Variations in the diode's performance as a doubler with its geometry and doping profile were analyzed for optimum efficiency and output power. Optimum doubler performance was obtained as a consequence of use of the optimized diode parameters resulting from this analysis. A simple but highly effective circuit topology was employed to transform the 50 Ω terminations to optimum source an load impedances, and also to provide isolation between the fundamental and second harmonic signals at input and output ports. Measured results of the diode parameters as well as doubler response showed excellent agreement with the analysis. The doubler exhibits better performance than those reported in the literature at similar frequencies using an MMIC approach.

I. INTRODUCTION

SCHOTTKY-BARRIER diode frequency doublers have been widely used as power sources at microwave and millimeter-wave frequencies to extend the frequency range of fundamental oscillators. Theoretical analysis of frequency doublers has been extensively investigated [1]–[3], revealing dependence of doubler performance on the varactor diode cutoff frequency, breakdown voltage, and diode input/output termination impedances. In millimeter-wave transmitter applications, where high power handling capability is required, series connected [4] and stacked varactor diode [5] doublers have been used to increase breakdown voltage. However, prior work did not provide detailed optimization of design parameters. In addition, the stacked varactor diode approach is difficult for MMIC implementation.

Alternatively, the varactor diode structure parameters can be optimized to exhibit higher cutoff frequency and breakdown voltage required for high efficiency and output power. The purpose of the present paper is to report on optimization of design parameters for single diode doublers, and to present supporting experimental data. In general, to achieve high cutoff frequency, a heavily doped, small, and thin epilayer is necessary for the diode,

which in turn limits the breakdown voltage, current flow, and hence the power handling capability. Moreover, the diode n^+ layer needs to be thicker than its skin depth to reduce series resistance. In this paper, junction capacitance, parasitic resistance, including spreading resistance and skin effect, and breakdown voltage of a disk-type varactor diode are analyzed. The optimized dimension and doping concentration are determined. Results of such analysis were used to develop a doubler circuit, which led to the state-of-the-art results for a 94 GHz MMIC frequency doubler.

II. DIODE ANALYSIS AND OPTIMIZATION

Fig. 1(a) shows the configuration of a conventional planar disk-type Schottky-barrier varactor diode commonly used for MMIC doubler design. Successful development of a doubler circuit hinges on proper design and accurate modeling of the varactor diode, which determine the intrinsic efficiency (conversion loss), and the maximum output power the doubler can achieve. The high-frequency model of a Schottky-barrier varactor diode consists of a resistance R_s, in series with the barrier admittance $(1/R_j + j\omega C_j)$, as shown in Fig. 1(b), where R_j is in the kΩ range so the capacitance dominates the admittance at sufficiently high frequencies. The series resistance R_s consists of voltage dependent epilayer resistance, spreading resistance and contact resistance. At millimeter-wave frequencies, skin effect has to be considered for maximum accuracy. For the mesa-type diode structure having both contacts on top of the chip, the current through the device has to flow down from the anode and spread laterally around the base of the mesa before flowing out of the cathode. Assuming the current density is confined parabolically within a skin depth δ, the series resistance R_s is broken into several components as shown in Fig. 1(c). The analytical equations for the diode parameters, based on previous work [6], [7], are given as follows:

$$R_n = \frac{t'}{\sigma_n \pi a^2} \tag{1}$$

where $t' = t - t_d$; t is the epilayer thickness and t_d is the depletion layer thickness. Under high power drive, R_n is

n Active Region

Schottky Contact Anode

n+ Substrate Region

Ohmic Contact Cathode

(a)

Rj

Rs

Cj

(b)

Schottcky Contact   **Ohmic Contact**

a

b

c

R_n

t

n

δ

h

n+

GaAs S.I.
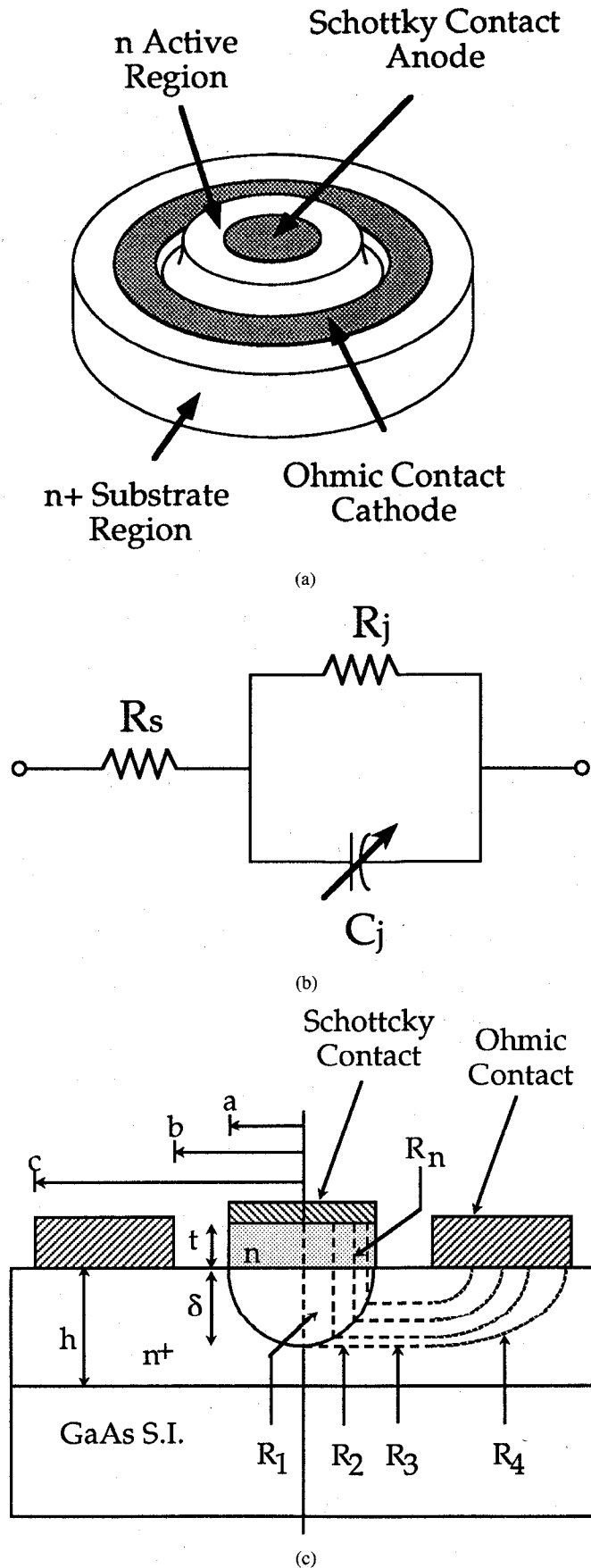
R_1 R_2 R_3 R_4

(c)

Fig. 1. (a) Planar disk-type Schottky-barrier varactor diode, (b) equivalent circuit of the diode, and (c) current flows through the diode and various components of the diode series resistance.

voltage dependent and this effect has to be taken into account.

$$R_1 = \frac{\delta_s}{2\sigma_s \pi a^2} \qquad (2)$$

$$R_2 = \frac{1}{4\pi\sigma_s\delta_s} \qquad (3)$$

$$R_3 = \frac{1}{2\pi\sigma_s\delta_s} \ln\left(\frac{b}{a}\right) \qquad (4)$$

$$R_4 = \frac{\rho_m \rho_s}{\rho_m\delta_s + \rho_s\delta_m} \left\{ \frac{1}{2\pi} \ln\left(\frac{c}{b}\right) \right.$$

$$+ \frac{\delta_s}{\rho_s} [AI_o(\beta c) + BK_o(\beta c)]$$

$$+ \left. \frac{\delta_m}{\rho_m} [AI_o(\beta b) + BK_o(\beta b)] \right\} \qquad (5)$$

where

$$A = \frac{1}{2\pi\beta\Delta} \left[\frac{\rho_m}{\delta_m c} K_1(\beta b) + \frac{\rho_s}{\delta_s b} K_1(\beta c) \right]$$

$$B = \frac{1}{2\pi\beta\Delta} \left[\frac{\rho_m}{\delta_m c} I_1(\beta b) + \frac{\rho_s}{\delta_s b} I_1(\beta c) \right]$$

$$\Delta = I_1(\beta c) K_1(\beta b) - I_1(\beta b) K_1(\beta c)$$

$$\beta = \left[\frac{1}{\rho_c} \left(\frac{\rho_m}{\delta_m} + \frac{\rho_s}{\delta_s} \right) \right]^{1/2}$$

ρ_c is ohmic contact resistance, δ_s and δ_m are skin depths, ρ_s and ρ_m are resistivities, σ_s and σ_m are conductivities, in the substrate and metal regions, respectively. $I_n(\cdot)$ and $K_n(\cdot)$ are modified Bessel functions of the first and second kind, respectively. The total series resistance of the diode is then given by $R_s = R_n + R_1 + R_2 + R_3 + R_4$.

The diode junction capacitance is given by

$$C_j = \frac{C_{j0}}{\sqrt{1 + \frac{V}{\Phi_0}}} \qquad (6)$$

where C_{j0} is zero bias junction capacitance and Φ_0 is the barrier potential. The breakdown voltage is expressed approximately by [8]

$$V_B = 60 \left[\frac{E_g}{1.1} \right]^{1.5} \left[\frac{10^{16}}{N_d} \right]^{0.75}. \qquad (7)$$

The doubling efficiency η and maximum output power P_{out} of an abrupt junction varactor diode can be predicted from the diode parameters by [1], [9]

where $C_{\min}$ is the junction capacitance at breakdown voltage V_B. The coefficients [10.4 in (8) and 0.0285 in (9)] were obtained by solving the nonlinear charge equation in the diode junction [1].

Variation of a varactor diode series resistance and cutoff frequency with the active layer doping concentration has been simulated and is shown in Fig. 2(a). Dou-
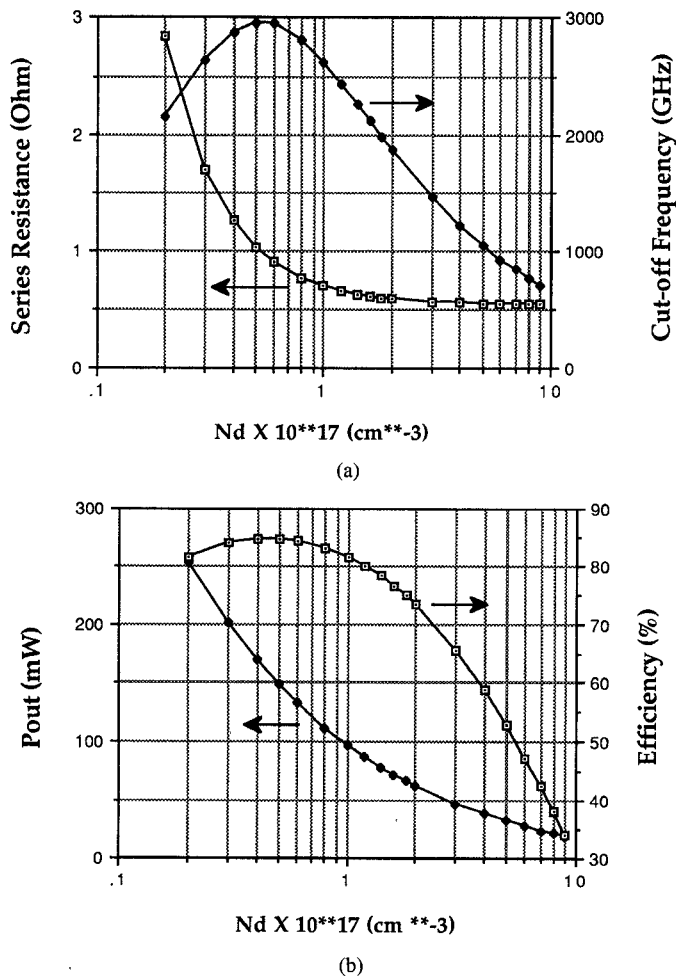
Fig. 2. (a) Series resistance and cutoff frequency, and (b) efficiency and output power as function of the active layer doping (Schottky contact diameter = 16 μm, n^+- layer thickness = 2.5 μm, and the active layer thickness is changed with the doping concentration to prevent depletion of the layer into the n^+ substrate at the breakdown voltage).

bling efficiency and maximum output power of the diode as a function of doping concentration are shown in Fig. 2(b). The figure shows that an optimum epilayer doping concentration exists for maximum efficiency which coincides with the maximum cutoff frequency.

III. DOUBLER DESIGN

The design of the 94 GHz frequency doubler started with an analysis of the diode structure as depicted above for optimized efficiency and output power at 94 GHz with 350 mW input at 47 GHz. Based on the results of the optimization, a varactor diode with a 16-μm-diameter Schottky contact and an active layer of 7×10^{16} cm^{-3} doping concentration were chosen for optimum efficiency as indicated by Fig. 2(b). The breakdown voltage of the diode was estimated to be 20.5 V. The thickness of the active layer was in turn determined to be 0.65 μm from the doping concentration and breakdown voltage so as to keep the depletion layer in the active region from penetrating into the substrate at full drive condition. By using the optimized diode doping profile, a zero-based cutoff

TABLE I
COMPARISON OF THE MEASURED AND PREDICTED DIODE PARAMETERS AND DOUBLER PERFORMANCE

Parameter	Value
Active Layer Doping	7×10^{16} cm^{-3}
n^+ Layer Doping	8×10^{18} cm^{-3}
a (see Fig. 1(c)	8 μm
b (see Fig. 1(c)	10 μm
c (see Fig. 1(c)	20 μm
Active Layer Thickness	0.65 μm
n^+ Layer Thickness	2.5 μm

	Predicted	Measured
Series Resistance R_s	0.82 Ω	0.87 Ω
Zero-Based Capacitance (C_{j0})	0.17 pF	0.17 pF
Breakdown Voltage (V_B)	20.5 V	18 V
Efficiency (η) at 330 mW Input	28.1 percent	19.7 percent
Output Power at 330 mW Input	93 mW	65 mW

frequency higher than 1100 GHz was achieved. Further parameters of the varactor diode together with measured results are shown in Table I.

Fig. 3(a) shows the configuration of the 94 GHz doubler circuit. Ideally, the input matching circuit is made transparent to the 47 GHz signal and shorts out all the harmonics generated by the nonlinearity of the diode; the output matching circuit allows maximum power at the second harmonic frequency being delivered to the load and rejects all other harmonics and the residual fundamental frequency power. This input and output isolation can be approximately achieved by adding a $\lambda/4$ short stub (of 47 GHz) and a $\lambda/4$ open stub (of 47 GHz) at the input and output side of the diode, respectively. Since $\lambda/4$ at 47 GHz is equivalent to $\lambda/2$ of 94 GHz, the short stub at the input side of the diode creates an RF short circuit at 94 GHz to prevent the output signal from traveling backward without affecting the impedance at 47 GHz. Similarly, the $\lambda/4$ (of 47 GHz) open stub at the output side of the diode generates an RF short at 47 GHz and causes the input signal penetrating through the diode to be reflected back without perturbing the impedance at 94 GHz. The resultant equivalent circuit with the $\lambda/4$ stubs is shown in Fig. 3(b). Since the diode is modeled as a voltage dependent capacitive impedance, inductive source and load terminations are required in order to resonate the diode junction capacitance to obtain maximum efficiency and output power. Theoretical analysis of source and load resistance, R_g and R_l, for optimum efficiency and output power has been investigated [1]-[3]. A simple approach to implement the input and output matching circuits, as shown in Fig. 3(d), is to use a section of transmission line as an inductor to resonate out the average diode junction capacitance and a $\lambda/4$ impedance transformer to transform 50 Ω to the optimum diode termination resistance.

It is worthwhile to note that the efficiency and maximum power predicted in Fig. 2(b) assumes full drive (at breakdown voltage V_B) and neglects circuit loss and other parasitic elements associated with the device and circuit.
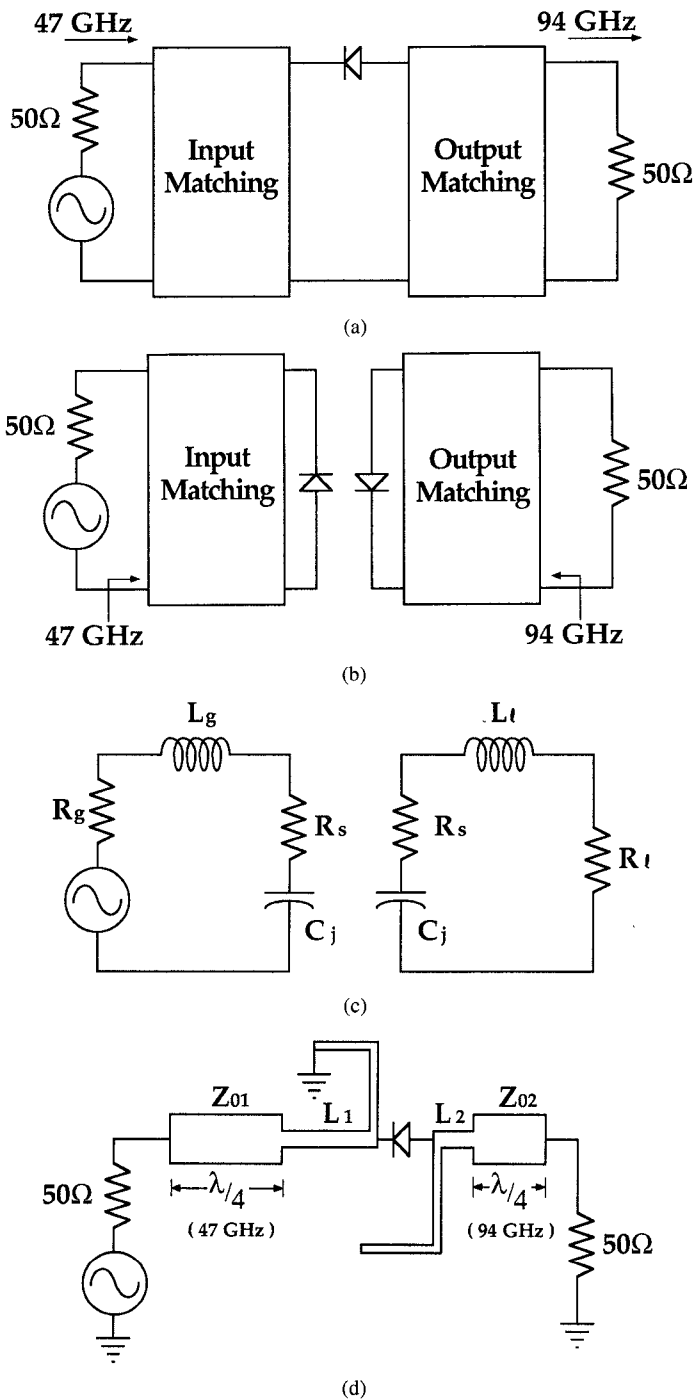
Fig. 3. (a) The 94 GHz varactor diode doubler circuit, (b) isolation between the input and output signals is achieved by using two $\lambda/4$ stubs at 47 GHz, (c) optimum inductive source and load impedance terminations are required for the diode to obtain maximum efficiency and output power, and (d) schematics of the 94 GHz doubler.

In addition, RF power of the third and higher harmonics generated by nonlinearity of the diode are ignored in the expressions. For accurate modeling of the doubler response, more rigorous time domain or frequency domain nonlinear circuit analysis, such as SPICE or LIBRA[1], is necessary. Nonetheless, the results predicted by (8) and

[1] Nonlinear simulation software, a trademark of EEsof.

(9) provide extremely valuable information on diode parameters for optimum doubler performance. Some parameters of the varactor diode, together with measured results, are given in Table I. Simulated results of a 94-GHz doubler in LIBRA using the diodes are also presented in the table. Excellent agreement of the predicted values with the measured results was achieved, and validity of the analysis was verified.

IV. FABRICATION AND MEASURED RESULTS

The 94 GHz doubler was designed using the approach described previously. Fig. 4 shows the microphotograph of the MMIC doubler chip, which was fabricated on a vapor phase epitaxy (VPE) substrate that has a buried n^+ layer to minimize the diode series resistance [10]. An Au/Ge/Ni/Ag/Au alloy was used for the ohmic contacts and Ti/Pt/Au metallization for Schottky-barrier contacts. Si_3N_4 was used for both the capacitor dielectric layer and chip passivation. Following completion of the circuits through the front side, via holes were etched in the thinned wafer. Gold was then plated onto the backside and via holes to a thickness of 10 μm prior to dicing the chips. The diodes had breakdown voltage exceeding 18 V.

High-performance waveguide-to-microstrip transitions are essential for accurate evaluation of the MMIC doubler chips at millimeter-wave frequencies. Ridged waveguide-to-microstrip line transitions were selected to provide rigidness and low insertion loss. Fig. 5 shows the MMIC doubler mounted on the test fixture consisting of a U-band and W-band microstrip to ridged waveguide transitions. The U-band transition has typical insertion loss of 0.25 dB and return loss better than 20 dB over the frequency from 40 to 48 GHz; and the W-band transition, including a section of 200 mil 50 Ω microstrip line on a 5 mil fused silica substrate, exhibits typical insertion loss of 0.6 dB and return loss better than 16 dB from 90 to 97 GHz. The measured output power and efficiency with input power ranging from 15 to 25 dBm are shown in Fig. 6. The reverse bias applied to the varactor diode was 7 V. The doubler exhibited a maximum efficiency of 25 percent (6 dB conversion loss) and output power of 55 mW at an input power of 220 mW. At an input level of 330 mW, 65 mW output power was obtained. The predicted output power and efficiency using LIBRA and the nonlinear diode model described in the previous section are also shown in the figure and exhibit very good agreement with the measured results.

V. CONCLUSIONS

Theoretical analysis and simulated performance of a Schottky-barrier varactor diode frequency doubler have been presented. Optimum diode parameters exist for optimum efficiency and output power and can be determined from analysis. A state-of-the-art 94 GHz doubler was designed and fabricated based on the results of the diode analysis and the use of a simple but effective circuit to-
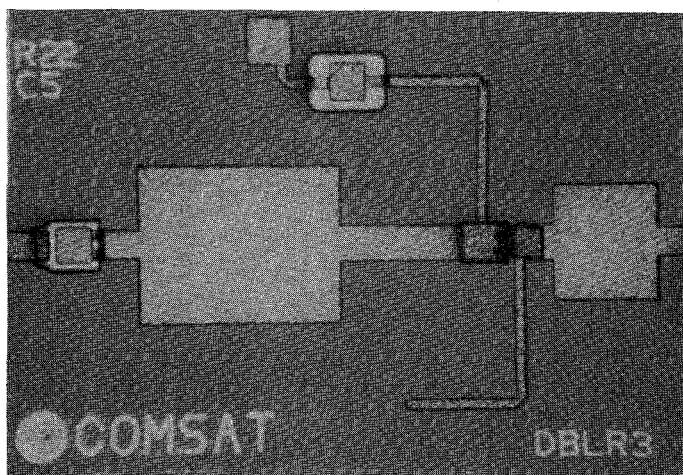
Fig. 4. Microphotograph of the 94-GHz MMIC frequency doubler (chip size 1.5 × 1.0 × 0.09 mm).
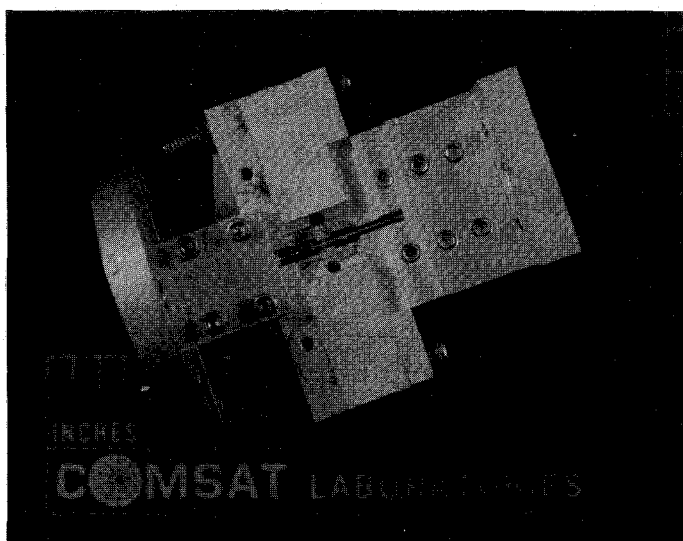

Fig. 5. Photograph of the MMIC doubler chip mounted on the test fixture with U-band and W-band ridged waveguide-to-microstrip line transitions.
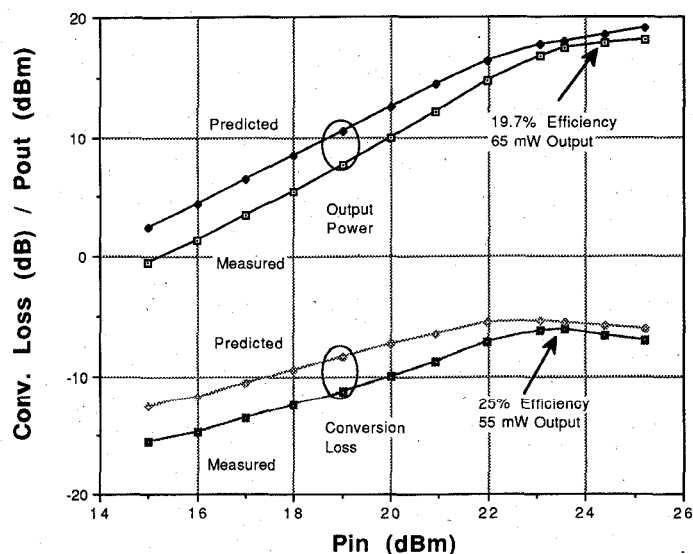

Fig. 6. Measured and predicted performance of the doubler.

pology. Measured results on the varactor diode and doubler showed excellent agreement with the predicted performance.

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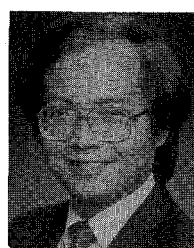
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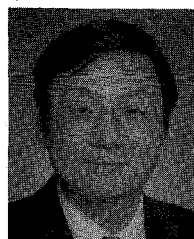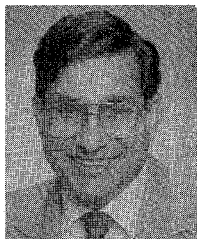
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